AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 1, lines 5-7, with the following paragraph:

This application is a Continuation of application No.09/410,772, Oct. 1, 1999, which ~~application~~ claims priority to S.N. 99400472.9, filed in Europe on February 26, 1999 (TI-27700EU) and S.N. 98402455.4, filed in Europe on October 6, 1998 (TI-28433EU).

Please replace the paragraph beginning on page 8, line 25 and ending on page 9, line 9, with the following paragraph:

In addition to being used for addressing, the self-timing logic is used for switching data that must be written in the memory core. Thus, the same process is used to latch the data that are output from the memory core. As an example, the self-timed signal "ordy" (output ready that is active low) can be used to latch the valid data from the core. In such an implementation, it is not necessary to use the system clock to latch the output data, as illustrated in FIG. 7. Moreover, using the access ready "accrdy" and the output ready "ordy" self-timing signals, it is possible to link up more than 2 access in a single cycle of the clock period if we assume for example that the signification of the rising edge of the "ordy" is the end of the cycle time of the memory. FIG. 8 illustrates the timing diagram of a triple access in one cycle. The system clock initializes the process after which the self-timing logic can link up accesses by itself without the help of the system clock. As a result, the accesses following the access synchronized on the system clock ~~to the core~~ are ~~fully~~ decorelated from the system clock.

Please replace the paragraph on page 9, lines 10-15, with the following paragraph:

The self-timing architecture of the present invention as applied to memory wrappers avoids calibration problems. Moreover, the self-timing logic of the present invention facilitates ~~a full~~ the dissociation from the system clock for the access following the access synchronized on the system clock, providing data to the core when needed ~~between the environment (what is clocked on the system clock) and the access to the core~~. A direct application is to make accesses at the speed of the core to process several accesses in one system clock cycle.

Replace the paragraph beginning on page 19, line 25 and ending on page 20, line 11, with the following paragraph:

DSP 190 also includes power distribution circuitry 224 for receiving and distributing the power supply voltage and reference voltage levels throughout DSP 190 in the conventional manner. As indicated in Figure 17, DSP 190 according to the preferred embodiment of the present invention may be powered by extremely low power supply voltage levels, such as on the order of 1 volt. This reduced power supply voltage is of course beneficial in maintaining relatively low power dissipation levels, and is in large part enabled by the construction and operation of PLL clock generator 222, which generates stable and accurate internal clock signals even with such low power supply voltages. In this emobodi~~bid~~ment of the invention, multiple access memory 26 is part of RAM 206, which means it is included in the processor core. Incorporation of multiple access memory 26 into the processor core facilitates increased accessing of the memory core and power savings since memory wrapper ~~since memory wrapper~~ 28 is eliminated and memory interface unit 48 is not used as an interface between the processing engine and the multiple access memory 26.